REMARKS

This is a timely reply to the Official Action of February 19, 2002. In the Official Action, the Examiner rejects pending claims 1-8 of the application. The grounds for rejection are traversed below. New claims 15-22 have also been added to the application.

Support for Amended claim 8 and New claims 15-21

Claim 8 has been amended to correct for antecedent basis. No new matter has been added. The breadth of amended claim 8 is the same claim 8 as originally filed.

Support for claim 15 can be found in Figures 1 and 2 and on pages 4-5 and page 8 of the present application. Support for claim 16 can be found on page 7. Support for claim 17 can be found on pages 8-9. Support for claim 18 can be found in Figure 3 and on page 6. Support for claim 19 can be found in Figures 1, 2 and 5 and on page 4-5 and 8-9. Support for claim 20 can be found on page 7. Support for claim 21 can be found on pages 8-9. Support for claim 22 can be found in Figure 3 and on pages 6 and 8-9.

Claims 1-8 remain in the application. Non-elected claims 9-14 have been canceled. The non-elected claims will be made the subject of a continuing application. New claims 15-22 have been added to the application. The application comprises 4 (four) independent claims and 16 (sixteen) total claims. The original application comprised 3 (three) independent claims and 14 (fourteen) total claims. The additional excess claims fees have been calculated as shown in the enclosed Excess Claim Fee paper.

USC § 103(a) - Rejection based on Choi (U.S. Patent No. 6,215,158)

Claim 1

In the Official Action, the Examiner rejects the claims of the application under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,215,158 to Choi. Specifically, the Examiner asserts that Choi teaches all of the elements found in claim 1 and the recitations of "a camouflaged interconnection" and "in a manner which inhibits reverse engineering thereof" in the claim preamble are treated as non-limiting.

As noted by MPEP 2143.03, to establish a *prima facia* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of Claim 1.

Choi teaches a memory device where during p-tub 120 formation, the interconnect layer 130 is formed by patterning and implanting the p-tub with an n-type dopant. After the p-tub 120 and interconnect layer 130 are formed, the first and second source regions 140, 150 and the drain region 160 are formed by conventional processes - see col. 3, lines 15-29. Thus, as is shown in Figures 1-4 and 6, the interconnect layer 130 is below the first and second source regions 140, 150.

Claim 1, on the other hand, recites "a first implanted region in the integrated or device forming a conducting channel between the two spaced-apart implanted regions". In the Official Action the Examiner states that the first implanted region of the present application corresponds to the interconnect layer 130 of Choi. However, Merriam-Webster's Collegiate ® Dictionary defines between as "in the time, space or interval that separates". Thus, the interconnect layer 130 of Choi is not between the first and second source regions. Interconnect layer 130 is not in the "interval (or space) that separates" the first and second implanted regions. Therefore, the interconnect layer 130 of Choi is not "a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions" as recited in claim 1 of the present application. The

Examiner is asked to point out where in Choi "a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions" is taught or suggested.

In addition, Choi teaches that a high energy beam of n-dopant is used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150, see col. 3, lines 39-43. Thus, Choi teaches that three implanted regions 231, 130, 232 are required in order to provide the connections from the first source region 140 to the second source region 150. Thus the interconnecting layer 130 is not "a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions" as is claimed in claim 1. Rather, Choi requires multiple implanted regions to perform this function. The Examiner is asked to point out where in Choi "a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions" is taught or suggested.

Further, claim 1 claims "a second implanted region of opposite conductivity type ... overlying said conducting channel". The Examiner asserts on page 3 of the Official Action that region 121 of Choi is the second implanted region. However, Choi teaches that implanted plugs 231 and 232, in addition to interconnect layer 130, are necessary to provide a conducting channel from the first source region 140 and the second source region 150. As can be seen in Figures 1-4 and 5 of Choi, region 121 does not overlay implanted plugs 231 and 232. Rather, implanted plugs 231 and 232 are implanted to overcome the second doped region 121. The Examiner is asked to point out where in Choi "a second implanted region of opposite conductivity type ... overlying said conducting channel" is taught or suggested.

The Examiner takes the position on page 4 that "the second doped region 121 of Choi inherently camouflages the buried interconnect 130 and inhibits reverse engineering." Applicant respectfully disagrees. Choi teaches that in order to connect

the first source region 140 and the second source region 150 dielectric 190 has to be patterned with openings 240, 250 respectively. Then a high energy beam of n-dopant is used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150. The openings 240, 250 are then filled with conductive plugs 440, 450 - see col. 3, lines 34-55. The reverse engineer will see the conductive plugs 440, 450 and know that the source regions have been connected. Therefore, the interconnection scheme of Choi is not camouflaged at all.

Since, for the reasons stated above, the interconnect layer 130 of Choi is not "a first implanted region in the integrated circuit or device forming a conducting channel between the two spaced-apart implanted regions" as is recited in claim 1 of the present application nor is region 121 of Choi "a second implanted region of opposite conductivity type ... overlying said conducting channel", claim 1 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 2-4 are also deemed to be patentable over the cited prior art through at least their dependency on claim 1.

Claim 5

As noted by MPEP 2143.03, to establish a *prima facia* case for obviousness, all the claim limitations must be taught or suggested by the prior art. The Applicant respectfully asserts that Choi does not teach all of the claim limitations of Claim 5.

Claim 5 claims in part "a plurality of interconnects ... each interconnect comprising a buried conducting channel bridging a region between the selected implanted regions". As stated above according to the definition of between, the interconnect layer 130 of Choi is not "a buried conducting channel bridging a region between the selected implanted regions" as is claimed in claim 1. The Examiner is asked to point out where in Choi "a plurality of interconnects ... each interconnect comprising a

buried conducting channel bridging a region between the selected implanted regions" is taught or suggested.

In addition, claim 5 claims " a buried conducting channel" and "at least one implanted region of opposite conductivity type being disposed over a least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" (emphasis added). Again as discussed in relation to claim 1, Choi teaches that implanted plugs 231 and 232, in addition to interconnect layer 130, are necessary to provide a conducting channel or interconnect from the first source region 140 and the second source region 150. As can be seen in Figures 1-4 and 5 of Choi, region 121 does not overlay implanted plugs 231 and 232. In addition, as can be seen from Figures 1-4 and 5 of Choi, the conducting channel (conducting layer 130, and plugs 231, 232) is not buried. The Examiner is asked to point out where in Choi " a buried conducting channel" and "at least one implanted region of opposite conductivity type being disposed over a least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" is taught or suggested.

Further, the Examiner takes the position on page 4 that "the second doped region 121 of Choi inherently camouflages the buried interconnect 130 and inhibits reverse engineering." Applicant respectfully disagrees. Choi teaches that in order to connect the first source region 140 and the second source region 150 dielectric 190 has to be patterned with openings 240, 250 respectively. Then a high energy beam of n-dopant is used to create implanted plugs 231, 232 thereby forming connections between the interconnect layer 130 and the first and second source regions 140, 150. The openings 240, 250 are then filled with conductive plugs 440, 450 - see col. 3, lines 34-55. The reverse engineer will see the conductive plugs 440, 450 and know that the source regions have been connected. Therefore, the interconnection scheme of Choi is not camouflaged at all. Thus, Choi does not teach or suggest "at least one implanted region of opposite conductivity type being disposed over a least a

majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" as is claimed in claim 5.

Since, for the reasons stated above, the interconnect layer 130 of Choi is not "a plurality of interconnects ... each interconnect comprising a buried conducting channel bridging a region between the selected implanted regions" nor is the second doped region 121 of Choi "at least one implanted region of opposite conductivity type being disposed over a least a majority of said plurality of interconnects to camouflage said at least a majority of said plurality of interconnects" as is recited in claim 5 of the present application, claim 5 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 6-8 are also deemed to be patentable over the cited prior art through at least their dependency on claim 5.

Patentability of New Claims

New claim 15 recites, " An interconnection scheme for interconnecting two spaced-apart regions of a common conductivity type in an integrated circuit or device in a manner which inhibits reverse engineering thereof, the interconnection scheme comprising: a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type, the first region providing a buried conducting channel for the two spaced-apart regions; and a second region of opposite conductivity type in the integrated circuit or device, said second region overlaying said first region to conceal the conducting channel." (empahsis added)

For reasons similar to those provided in support for the patentability of claims 1 and 5, Choi does not disclose "a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type", a "first region providing a buried conducting channel" or a "second region overlaying said first region to conceal the conducting channel" . The Examiner is asked to point out where in Choi "a first

region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type", a "first region providing a buried conducting channel" or a "second region overlaying said first region to conceal the conducting channel" is taught or suggested.

Since the interconnect layer 130 of Choi is not a first region in the integrated circuit or device disposed laterally of and in direct contact with the two spaced-apart regions, the first region being of said common conductivity type", nor a "first region providing a buried conducting channel" and since the second doped region 121 of Choi is not a "second region overlaying said first region to conceal the conducting channel" as is recited in claim 15 of the present application, claim 15 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 16-18 are also deemed to be patentable over the cited prior art through at least their dependency on claim 15.

New claim 19 recites, "A interconnection scheme for interconnecting a plurality of spaced-apart regions of a common conductivity type in an integrated circuit or device, the interconnection scheme comprising: a plurality of buried conducting channels, each buried conducting channel being of the common conductivity type, each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions, each buried conducing channel providing an electrical connection between said selected ones of the plurality of spaced-apart regions; and at least one region of an opposite conductivity type in the integrated circuit or device, the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels." (emphasis added)

For reasons similar to those provided in support for the patentability of claims 1 and 5, Choi does not disclose " a plurality of buried conducting channels", each buried

conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions" nor "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels". The Examiner is asked to point out where in Choi "a plurality of buried conducting channels", each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions" or "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels" is taught or suggested.

Since the interconnect layer 130 of Choi is not "a plurality of buried conducting channels", each buried conducting channel being laterally disposed of and in direct contact with selected ones of the plurality of spaced-apart regions" and second doped region 121 of Choi is not "the at least one region of opposite conductivity type being disposed over at least a majority of said plurality of buried conducting channels to camouflage said at least a majority of said plurality of buried conducting channels" as is recited in claim 19 of the present application, claim 19 is clearly distinguishable over Choi, and therefore deemed to be patentable. In addition, claims 20-22 are also deemed to be patentable over the cited prior art through at least their dependency on claim 19.

Conclusion

Hence, the Applicant respectfully submits that all claims of the application are patentable over the cited references. In view of the above, reconsideration and allowance of the pending claims are respectfully solicited.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this

response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231 on

May 20, 2002
(Date of Deposit)

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APPENDIX A

IN THE CLAIMS

8. (Once Amended) The invention of claim 5 wherein the [second implanted region] at least one implanted region of opposite conductivity type is provided in said integrated circuit or device over regions having no conducting channels formed therein.

IN THE SPECIFICATION

The first paragraph under the Detailed Description on page 4:

Figure 1 is a cross sectional view through a portion of a two interconnected active devices 1, 2 in an integrated circuit. Only a portion of two active devices are shown in Figure 1 since this invention is concerned with techniques for camouflaging the interconnections rather than with the structure of the devices *per se*. The depicted portion of active device 1 [which is depicted] is a N-type region 11 [which] that could provide the drain, for example, of a first FET transistor 1 and could be formed as an implanted region with a N-type dopant by techniques very well known in the art. Those skilled in the art will recognize, of course, that the N-type region 11 could alternatively form a portion of a diode, a portion of a bipolar transistor or a portion of some other semiconductor structure. The depicted portion of active device 2 [which is depicted] is a N-type region 12 [which] that could form the source, for example, of a second FET transistor 2. The function or functions attributed to regions 11 and 12 are not particularly important to the present invention and they could represent any implanted semiconductor structure as a matter of design choice.

The paragraph spanning pages 4 and 5:

A complicated integrated circuit can literally comprise millions of active regions. Of course, not all active regions or devices are connected to an immediately adjacent active region or device although that is not infrequently the case. With respect to

Figure 1, it is assumed that active region 11 and active region 12 require, due to the design of the integrated circuit device in which they are used, interconnection. In the prior art, they might well have been interconnected by providing a thin layer of gold, aluminum or other metallic conductor on the presently exposed surface 15 between implanted regions 11 and 12. However, according to the present invention, regions 11 and 12 are interconnected by a N-type implanted region 13 which provides a conduction channel that interconnects the two active regions 11, 12. In order to camouflage the N-type implant 13, an implant of opposite conductivity type, for example, an implant of P-type conductivity[type here,] is implanted in a shallower region 14 immediately above the conductive channel formed by region 13.

The first full paragraph on page 5:

Those skilled in the art will realize that, if the P-type implant 14 were not employed, [that] the N-type implant 13, which has a tendency to [would tend] extend towards the surface 15 of the semiconductor device shown in Figure 1, might be discoverable by stain and etch techniques. Depending on the type of implantation used, the concentration of the N-type dopant could [well] be higher in regions below surface 15 compared to regions immediately adjacent surface 15. The relatively deeper N-type implant 13 provides a conduction path and will most likely have a relatively high dose of dopant to form the implant (for example, the amount of dosage of the dopant in the conduction path implant 13 could be the same as the dosage used to implant the active regions 11 and 12). The camouflaging implant, namely[,] implant 14, is also a relatively heavy implant, in order to camouflage the opposite conductivity type material in region 13 forming the conducting channel. However, the camouflaging implant 14 is relatively shallow compared to the depth of the conducting implant 13.

The paragraph spanning pages 6 and 7:

The configurations shown in Figures 1 and 3 will be repeated over and over again on a semiconductor chip, possibly more than a million times depending upon the complexity of the chip. Indeed, the camouflaging implant 14, 24 may be used over essentially 100% of the area of the chip dedicated for use as interconnections and where interconnections between active regions could plausibly occur, but do not occur. As such, said camouflaging implant 14, 24 preferably has a larger area, when viewed in a direction normal to a major surface of [in] the integrated circuit or device, than the area of the conductive channels camouflaged thereby. If the reverse engineer can not infer the presence of a conductive channel merely by the presence of the camouflaging implant 14, 24, it makes the reverse engineer have to work all that much harder to try to determine just how the active regions in an integrated circuit are interconnected. Given the fact that there can be millions of interconnections and even more places where an interconnection could exist (but does not due to the particular requirements of the circuitry on the integrated circuit chip), this invention makes it impracticable for the reverse engineer to try to work out just where the interconnections do exist.

The paragraph spanning pages 8 and 9:

Figure 5 is a plan view of a small portion of an IC. Four FET transistors T1 - T4 are depicted together with the drains D1 - D4, sources S1 - S4 and gates G1 - G4. Drain D3 and source S4 are depicted as being interconnected by a buried implant 13-1. Drain D4 and source S2 are depicted as being interconnected by a buried implant 13-2. The regions in which interconnections could plausibly occur, but do not occur, and the regions over[-]lying buried interconnects 13-1 and 13-2 are all covered with a camouflaging implant 14, 24. As previously indicated, camouflaging implant 14, 24 is preferably implanted during a single implant process and is only given [a] different numerals herein to differentiate when it overlies an interconnect ([where it is] labeled [by] numeral 14) and when it overlies regions where interconnections

could plausibly occur, but do not occur ([where it is] labeled [by] numeral 24). The regions where buried interconnection 13 do or do not occur [and do not occur is] are governed by the particular function or functions to be performed by the IC in question. In the embodiment of Figure 5 it is clear that the camouflaging implant 14, 24 has a significantly larger area, when viewed in a direction normal to a major surface 15 (See Figures 1 & 3) of [in] the IC, than the area of the conductive channels 13-1 and 13-2 camouflaged thereby.